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№ 1796

An Efficient Dual Band 900MHz / 2.45GHz RF Energy Harvester

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October 31, 2019

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***Abstract*—Ambient Radio Frequency (RF) energy harvesting has been an attractive area of research due to its eventual applications in many modern low-power systems. The RF waves are present on several high frequency and at low power (a few µW). We present in this paper a new architecture RF-DC rectifier circuit operates at dual simultaneous frequencies. The bands frequencies chosen for this work are GSM (900MHz) and WIFI (2.45GHz). The proposed rectifier is designed in three stages using the MOSFET transistors, the capacitors and the inductors. The technology used is CMOS 0,18µm from TSMC and the simulations were performed using the ADS (Advanced Design System) Simulator. This circuit provides a Power Conversion Efficiency (PCE) of 68.4 % with an input power P_{in}= -21.3 dbm and an output voltage V_{out}=1.67 V for the frequency 900 MHz and a PCE of 72.4 % with an input power P_{in}= -20.5 dbm and an output voltage V_{out}=1.7 V for the frequency 2.45GHz.**

Keywords—Energy harvesting, ambient RF, dual band, RF-DC rectifier, LCLC, diode-connected MOSFET transistor.

I. INTRODUCTION

The aim of this work is to design a rectifier circuit that operates at 900 MHz and 2.45 GHz simultaneous and which receives a low power energy to convert it into DC voltage >1V. The voltages $V_{RF(rms)}$ of RF waves are very small of the order of a few mV. The MOSFET transistors cannot operate with very low voltages. Therefore, we have designed our circuit to work as a resonance tank that increases RF input voltages V_{RF_in}. This circuit is a combination series-parallel of an Inductor-Capacitor-Inductor-Capacitor (LCLC). A high AC voltage V_{boost} that occurs from this resonance tank. Transistors become into conduction and therefore our circuit works as a charge pump to finally have a DC voltage V_{out}.

The functional diagram of the proposed model rectifier is presented in Fig. 1. This model works in different frequency bands by acting on the values of the circuit components (capacitors, inductors and MOSFET transistors).

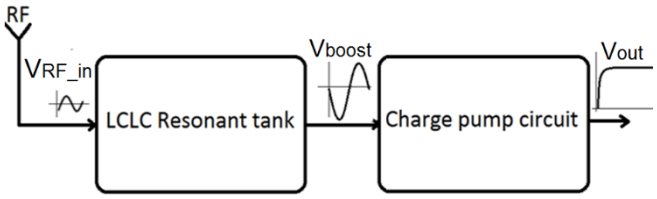

Fig. 1. Functional diagram of the proposed model rectifier

The paper is arranged as follows: the RF-DC circuit design methodology is discussed in Sec. 2, LCLC resonant tank and AC-AC boosting mode is showed in Sec. 3, after that the AC-DC charging pump mode is depicted in Sec.4 whereas the simulations and results are presented in Sec.5 and finally this article is completed by a conclusion in Sec. 6.

II. THE RF-DC CIRCUIT DESIGN METHODOLOGY

The proposed circuit rectifier RF-DC with n stages formed by NMOS and PMOS transistors is presented in Fig. 2.
Where C_{s1}, C_{s2},..,C_{s2n} are the pumping capacitors, C_{sr} and L_{sr} are the capacitor and inductor respectively placed in series at the beginning of the circuit, L_{pr_1},L_{pr_2},..,L_{pr_n-1} are the loading inductors, C_L is the load capacitor, R_L is resistor load and r is the resistor of the RF input signal.

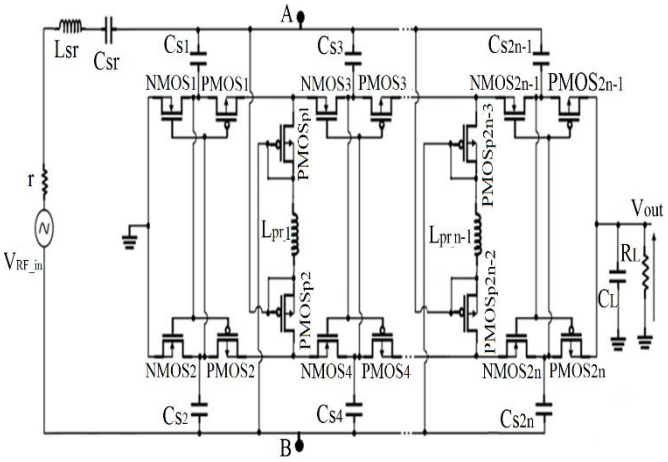

Fig. 2. The proposed circuit rectifier RF-DC

In view of the RF input power is very low as mentioned previously, the MOSFET transistors cannot operate with very low voltages. The proposed circuit operates with two operating modes. In the first mode (Fig. 3), all transistors are blocked, our circuit operates as a LCLC Serie-Parallel Resonant Tank (LCLC_SPRT) [1] to boost the AC input voltage [3]. In the second mode (Fig. 4), the transistors go into conduction, therefore the circuit operates as a charge pump [4]. Therefore, from an AC voltage, a DC voltage is generated.

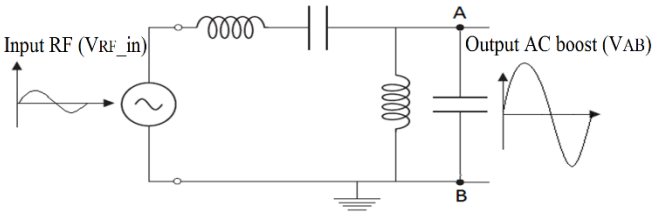

Fig. 3. Operating type of the circuit in "LCLC resonant tank and AC-AC boosting" mode

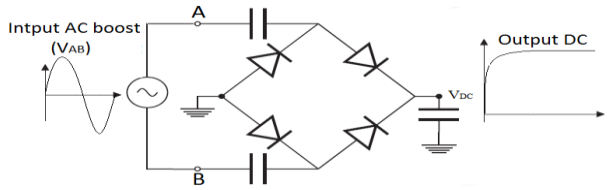

Fig. 4. Operating type of the circuit in "AC-DC charging pump" mode

III. "LCLC RESONANT TANK AND AC-AC BOOSTING" MODE

The equivalent circuit proposed on the "LCLC resonant tank and AC-AC boosting" mode is presented in Fig.5. Where the L_{sr} is the inductor serie resonant, the C_{sr} is the capacitor serie resonant, the L_{pr} is the equivalent parallel inductors of L_{pr_1}, L_{pr_2},…, L_{pr_n-1} and the C_{rec} is the equivalent capacitance of the rectenna circuit that is composed of the capacitors C_s and the equivalent capacitors of the NMOS and PMOS transistors (in blocked mode) used in the proposed circuit. A mathematical approach followed by a computer program to determine the component values and resonance frequencies are presented.

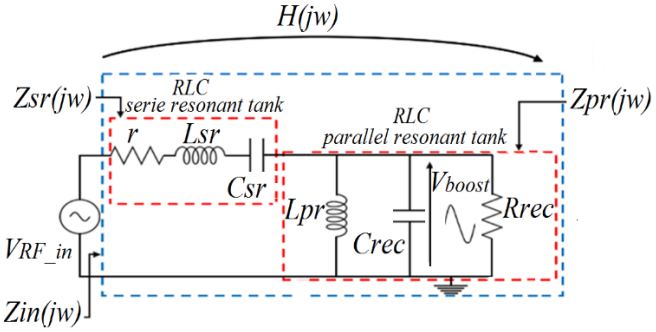

Fig. 5. LCLC serie parallel resonant tank circuit

A. Calculation of the gain and resonant frequencies

The transfer function of the LCLC tank is written in the form:

$$H(j\omega) = \left| \frac{V_{boost}}{V_{RF_{in}}} \right| = \frac{Z_{pr}(j\omega)}{Z_{in}(j\omega)} \quad (1)$$

Where Z_{in} is the input impedance, Z_{pr} is the impedance of RLC parallel resonant tank, V_{RF_in} represents the RF input voltage of the circuit proposed and V_{boost} is the AC output voltage of the LCLC_SPRT circuit.

By replacing the impedances of equation (1) by their components, we find the following transfer function:

$$H(j\omega) = \frac{1}{j\left(\frac{\omega L_{sr}}{R_{rec}} - \frac{1}{\omega C_{sr} R_{rec}} + r\omega C_{rec} - \frac{r}{\omega L_{Pr}}\right) + \frac{L_{sr}}{L_{pr}} + \frac{C_{rec}}{C_{sr}} - \omega^2 L_{sr} C_{rec} - \frac{1}{\omega^2 L_{pr} C_{sr}} + \frac{r}{R_{rec}} + 1} \quad (2)$$

The amplitude of the AC gain is done by (3):

$$|H| = \frac{1}{\sqrt{\left(\frac{\omega L_{sr}}{R_{rec}} - \frac{1}{\omega C_{sr} R_{rec}} + r\omega C_{rec} - \frac{r}{\omega L_{Pr}}\right)^2 + \left(\frac{L_{sr}}{L_{pr}} + \frac{C_{rec}}{C_{sr}} - \omega^2 L_{sr} C_{rec} - \frac{1}{\omega^2 L_{pr} C_{sr}} + \frac{r}{R_{rec}} + 1\right)^2}} \quad (3)$$

The LCLC_SPRT circuit comes into resonance when the real part of the denominator of equation (2) equals zero:

$$\frac{L_{sr}}{L_{pr}} + \frac{C_{rec}}{C_{sr}} - \omega^2 L_{sr} C_{rec} - \frac{1}{\omega^2 L_{pr} C_{sr}} + \frac{r}{R_{rec}} + 1 = 0 \quad (4)$$

Equation (4) gives two frequencies of resonances (f_1 ; f_2) of the LCLC_SPRT circuit.

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{A - \sqrt{A^2 - 4B}}{2B}} \quad (5)$$

And

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{A + \sqrt{A^2 - 4B}}{2B}} \quad (6)$$

Where $\omega = 2\pi f$; $A = L_{sr}C_{sr} + (\frac{r}{R_{rec}} + 1)L_{pr} C_{sr} + L_{pr}C_{rec}$; $B = L_{sr} C_{sr} L_{pr} C_{rec}$; $A^2 - 4B > 0$ and $f_1 < f_2$.

B. Determining values of capacitors, inductances and resonance frequencies

We have developed a computer program with the Visual Basic (VB) using equations (4), (5) and (6) previously described to determine in practice the values of the components of the LCLC circuit as well as the resonance frequencies with a high amplitude of the boosted voltage V_{boost}.

Fig. 6 shows the interface of the program developed.

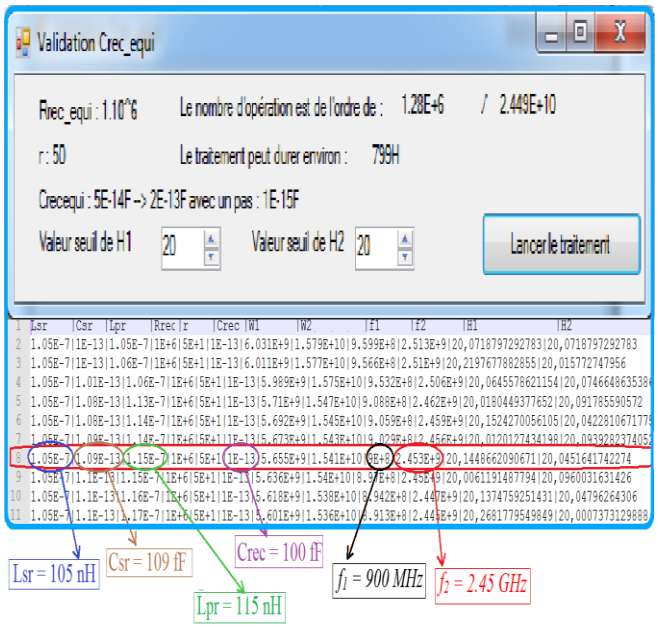

Fig. 6. Interface of the program developed and an extract of result of calculation for an example

The program works as follows:

First, Put the intervals and step of the values of each component: $L_{sr}=[L_{sr1},..,L_{srn}]$, $C_{sr}=[C_{sr1},..,C_{srn}]$; $L_{pr}=[L_{pr\_1},\ldots,L_{pr\_n}]$ and $C_{rec}=[C_{rec\_1},\ldots C_{rec\_n}]$. Then, Choose the threshold values of the amplitudes of the AC gain (H_1, H_2). Finally, start the process to display the possible values of the two resonant frequencies (f_1; f_2) with the values of the circuit components as well as the gain in amplitude.

We have used a threshold of 20 for H1 and H2 amplitude gains. An extract of the result is presented in Fig.6. The frequencies chosen for this work are f_1 = 900MHz and f_2 = 2.45GHz. The values of the components obtained are: Lsr = 105 nH, Csr = 109 fF, Lpr = 115 nH and Crec = 100 fF.

IV. "AC-DC CHARGING PUMP" MODE

In "AC-DC charging pump" mode, the circuit operates with the voltage V_{boost} provided by LCLC and therefore the transistors go into conduction.

The performance of charge pump circuit is improved by combining the Internal threshold Voltage Cancellation (IVC) [2] in the Dynamic threshold Voltage Cancellation (DVC) [3] circuit to reduce the threshold voltage and also using the technique of cascade arrangement [4] to improve the DC output voltage in each stage of the rectifier. This circuit is based on the connection of the transistors to each other in order to have a better DC output voltage V_{out}. The voltages threshold V_{thn} and V_{thp} decrease the output voltage V_{out}. So the integration of voltages between drain and gate in NMOS and PMOS transistors ($V_{gd} < 0$ for PMOS and $V_{gd} > 0$ for NMOS) reduces efficiently the voltages threshold V_{thn} and V_{thp} [5].

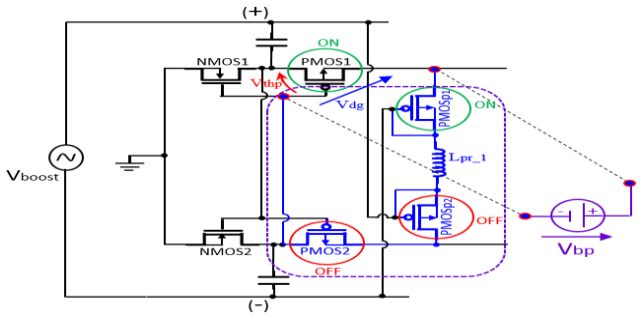

Fig. 7. Part of the proposed circuit with auxiliary voltage Vbp

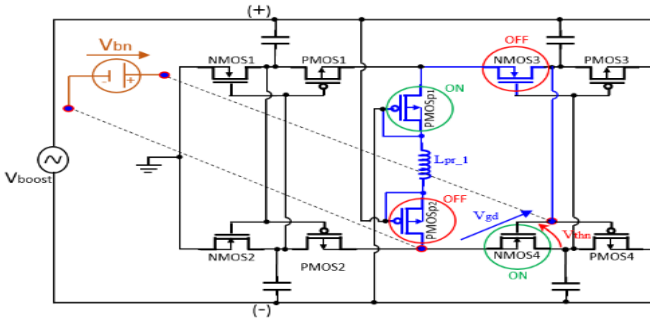

Fig. 8. Part of the proposed circuit with auxiliary voltage Vbn

Fig.7 and Fig.8 present the auxiliary voltage Vbp and Vbn for one half-wave. This additional voltage Vbp (Vbn) proposed is generated from a blocked transistor $PMOS_2$ ($NMOS_3$) and $PMOS_{p2}$, a transistor PMOSp1 in conduction and an inductance L_{pr_1} that is mounted opposite the drain and the gate of another transistor in conduction PMOS1 ($NMOS_4$). Indeed, $PMOS_1$, $PMOS_{p1}$ and $NMOS_4$ operate in conduction-mode. However, $PMOS_{p2}$, $PMOS_2$, and $NMOS_3$ are in cut-off mode. L_{pr_1} represent a load inductance. When the capacitor Csd (internal capacitance between source and drain) of $PMOS_{p1}$ transistor is loaded, the current reduces in the L_{pr_1}. When the capacitor Csd of $PMOS_{p1}$ transistor is almost at its maximum charge, the magnetic field in the coil collapses. This produces a reverse voltage in the L_{pr_1} inductance. So, L_{pr_1} acts as an additional voltage that represents the first auxiliary voltage. In addition, we have a second auxiliary voltage coming from the voltage produced by the source-to-gate (Vsg) of the diode-connected transistor PMOSp1 that will be added to the first auxiliary voltage.

We have calculated the output voltage V_{out} in this charging pump with n stages (See equation (7)):

$$V_{out} = (4n+2)V_{boost} - n[(V_{thn} - V_{bp}) + (V_{thp} - V_{bn})] - (V_{thn} + V_{thp}) \quad (7)$$

V. SIMULATIONS AND RESULTS

The circuit proposed is composed of three stages that is enough to have the desired DC voltage >1V. The simulation prelayout is made by ADS (technology CMOS 0.18µm

TSMC) at f_1= 900MHz and at f_2= 2.45GHz. The values of the components used in the circuit are as follows: $C_{s1}=C_{s2}=C_{s3}=C_{s4}=C_{s5}=C_{s6}$=8pF; L_{sr} = 105 nH; C_{sr} = 109 fF, L_{pr} = 115 nH; W_{NMOS}=4µm; W_{PMOS}=12µm; W_{PMOSp} = 30µm; C_L = 5pF. We have taken into consideration when designing and simulations of the circuit, the resistances of the components of the circuit and the parameters of the transistors manufacturing process (Ad, As, Pd and Ps). Fig.9 presents V_{in}, V_{boost} and the output voltage V_{out} extracted for the dual frequencies f_1= 900MHz and f_2= 2.45GHz with the RF inputs power Pin =-21.3 dbm and -20.5 dbm respectively.

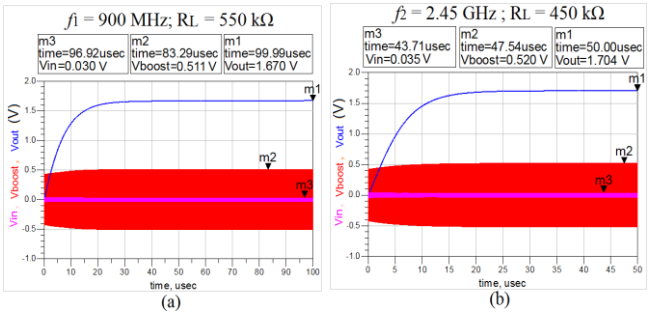

Fig. 9. Output voltage (Vout) (a) at f_1 = 900 MHz and (b) at f_2 =2.45 GHz

In order to verify the performance of the proposed circuit, it is necessary to calculate the Power Conversion Efficiency (PCE). The PCE can be expressed as follows:

$$PCE(\%) = \frac{P_{out\,(W)}}{P_{in(W)}} * 100 \qquad (8)$$

Where

$$P_{in(W)} = \frac{V^2_{in,rms\,(V)}}{r_{(\Omega)}} \qquad (9)$$

where r = 50 Ω,

and $$P_{out\,(W)} = \frac{V^2_{out\,(V)}}{R_{L\,(\Omega)}} \qquad (10)$$

Fig.10 presents the curves of the efficiencies PCE and the output voltages V_{out} in according to RF input power (P_{in}) at the dual frequencies f_1= 900 MHz and f_2= 2.45 GHz.

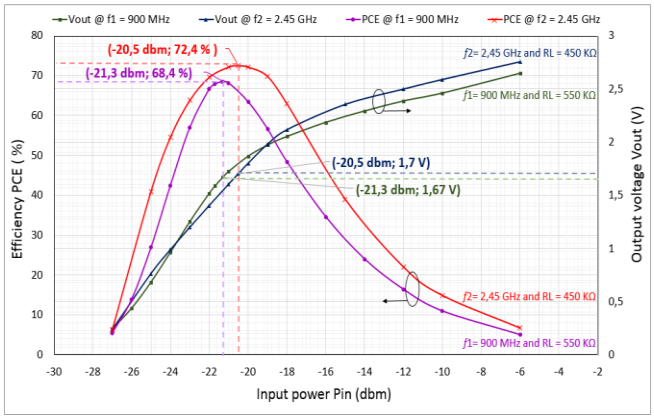

Fig. 10. Efficiency (PCE) and Output voltage (Vout) in according to input power (Pin) at the dual frequencies f_1= 900MHz and f_2= 2.45GHz

Table 1 shows a comparison between the proposed circuit and other circuits operating in dual frequencies. Overall, our circuit offers the best PCE and higher output voltages for lower RF input signals compared to other systems.

TABLE I. COMPARISON BETWEEN THE PROPOSED CIRCUIT AND OTHER CIRCUITS FOR DUAL FREQUENCIES

Ref.	CMOS used	Freq.	Pin (dbm)	R_L	Vout (V)	PCE (%)
This work[s]	0.18µm	900 MHz	-21.3	550 kΩ	1.67	68.4
		2.45 GHz	-20.5	450 kΩ	1.7	72.4
[6][m]	0.18µm	953 MHz	-14	60 KΩ	1.1	53.4
		2.4 GHz	-14	60 KΩ	1.1	55.7
[7][m]	0.065µm	1 GHz	-14.5	30 KΩ	1.3	25
		2.4 GHz	-14.5	1 KΩ	1.1	42
[8][s]	0.065µm	900 MHz	-19	1 MΩ	1.3	13.8
		2.4 GHz	-19	1 MΩ	1.44	16.8

$[X]_m$: measured results. $[X]_s$: simulation results.

VI. CONCLUSION

This paper presents a novel design of RF-DC rectifier operates in dual frequency simultaneously. In this work, the proposed circuit operates in two mode "AC-AC boosting" and "AC-DC charging pump".

The simulations are performed on the circuit proposed with an input power Pin = -21.3dbm and R_L=550 kΩ at f_1= 900MHz, the PCE found is 68.4 % and with an input power Pin=-20.5dbm and R_L=450 kΩ at f_2= 2.45GHz, the PCE found is 72.4 %.

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