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Dual Active Bridge - Based Battery Charging for EV with Charging Current Canceling Double Line Frequency Ripple

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***Abstract*—Two-stage single-phase rectifiers, which comprises a front-end ac-dc converter and a downstream DC-DC stage, are widely used in electric vehicle onboard charger applications. In this context, the implementation of bidirectional power transfer capabilities has gained considerable attention. Then, Totem-pole power factor correction and Dual Active Bridge converters emerge as commendable choices for enhancing the efficiency of this configuration. The incorporation of wide band gap semiconductor devices serves to elevate the switching frequency, resulting in a notable reduction in the dimensions of passive components. The size of passive components are then reduced significantly. However, the bulk DC-link capacitors of the AC-DC stage becomes one of the major barriers to achieve higher power density. The reason is their volume depend on the ripple power at the double line frequency, which generated from the AC-DC stage. Moreover, the charging current containing this low frequency ripple causes negative effect to the batter such as, more heat and reducing the battery life. To solve these problems, software technique to reduce this low frequency current ripple is studied. The analysis, simulations, and experiments are done to verified the effective of method. The results demonstrate that the output current ripple can be reduced by about 9 times when the control technique is applied.**

***Index Terms*—Totem-Pole Power Factor converter, Dual Active Bridge converter, double line frequency current ripple.**

I. Introduction

The recent proliferation of Electric Vehicles (EVs) has created significant interest in developing the technology around the on-board charger (OBC) applications. It is well-known as two stages including: AC-DC stage and DC-DC stage. The first AC-DC stage is used to work with the grid in which the power is converted from the AC to DC. Moreover, it makes the power factor (PF) and total harmonic distortion (THD) to satisfied some standard such as, IEC61000-3-2 [1]. The output of the PFC stage is feed to DC bus including a bank of capacitors. Then, it converts the DC power to the require power from battery's EV. The general requires of OBC are not only high efficiency and high power density, but the output charging current also need to be as smooth as possible. Moreover, the bidirectional function is also a promising trend to make an EV can be a source and transfer power back in case of need.

With the fast development of wide band gap devices, the converter switching frequency can be such increased to reduce the size of the passive element, such as the magnetic elements, the input or output filter. However, at the first PFC stage, there is always a second harmonic element (i.e 100 Hz) appearing at its output. When this low frequency ripple is increased, in the converter point of view, the stress currents power switches and magnetic components are then also increased. Hence, this ripple can reduce the energy conversion efficient of the system. From load requirement, the amplitude of peak-peak ripple is also increased which can be violated some standard such as, IEC61851-23 [2], CHAdeMO, etc. It also reduces the lifetime of bat load as, the battery and fuel cells. Therefore, the double line frequency ripple need to be solved. In this study, the battery heath is the main concern. Then, the solutions are focusing on the quality of charging current, and others using another active components such as power decoupling circuit are not preferred.

Due to the relatively low frequency, a large bank of electrolytic capacitors is required to be added to the DC bus. This results in high costs and wasted space, ultimately reducing the power density of the converter significantly [3]. Furthermore, these capacitors are the critical elements that limit the life time of the system. Following [4], the lifespan of a high-quality electrolytic capacitor is only 3000 to 5000 hours and declines by half with every temperature increase of 10^o C [5]. Based on that, using the huge bank capacitors is not a good solution.

Another solution is using the DC-DC stage to process the double line frequency. The controller of the DC-DC stage is carefully designed to canceled out the ripple. The similar ideal used to describe in the previous works [3], [6]. However, the power flow is transferred from the Battery to the grid and the effort is eliminated the ripple at the DC bus. Therefore, it can not be applied when the OBC operated at the CC mode.

In this paper, the ripple of the load current is con-

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trolled to achieve the flat charging current. The conventional proportional-integral (PI) controller is still used with the support of resonance (R) controller to achieve the goal. The PI controller is used to regulate the DC current to the desired value because it can be achieved high gain at DC. The AC ripple current can be canceled by using the R term in which the resonance frequency is set to the desired cancel frequency (or the double line frequency). Because of the ripple is processed at the DC-DC stage. Therefore, the Dual Active Bridge converter is used to implement this controller. Another converters can also used with the the same idea.

The rest of this paper is structured as follows: Section II describes the system configuration and assumptions. The modeling analysis of the Dual Active Bridge converter is presented Section III. Section IV shows the controller design with the low frequency ripple cancellation. The simulation results are depicted in Section V. Finally, the conclusion is summarized in Section VI.

II. System Configuration and Assumptions

A. Overview of the two stages single-phase rectifier

Fig. 1 shows the general structure of an onboard charger (OBC). It is composed of a PFC stage, a DC-link capacitor, and DC-DC stage. The first stage is PFC that converts an AC input to a fix DC-link voltage. The second stage is the isolated DC-DC converter, which transfers power for battery charging. Between these two stages, the DC-link capacitors are located to absorb the AC power generated from the PFC stage. Therefore, only DC power is transferred to the DC stage, ideally.

In order to make the OBC can be function bidirectional, the totem-pole PFC converters [7] are used for the first stage and the second stage widely uses the Dual Active Bridge (DAB) converters [8], [9]. The system diagram is demonstrated by Fig. 2. Ideally, the AC voltage from the grid supply power for the input of PFC with the fixed frequency (i.e. 50 Hz). Therefore, the output power from the first stage can be determine by Equation (1).

$$\begin{aligned} P_{bus} &= P_{dc} + P_{ac} \\ &= \sqrt{2}V_{ac}sin(\omega_0 t) \times \sqrt{2}I_{ac}sin(\omega_0 t) \\ &= VI(1 + cos(2\omega_0 t)) \end{aligned} \tag{1}$$

where, P_{dc}, and P_{ac} are the DC and AC-ripple power as mentioned above, respectively. V_{ac}, and I_{ac} are the AC input voltage and current, respectively, and ω_0 is the line frequency. As this equation shows, there is always the double frequency ripple (i.e. 100 Hz) at the DC bus (output of the PFC stage). The high amplitude of this ripple can have a significant impact on the DAB stage. Specifically, the output charging current also contains the low frequency ripple. This not only affects battery life but also violates the quality of the charging current according to some international standards, IEC61851-23 or CHAdeMO. Normally, this ripple frequency is filter by the capacitor as shown in Fig. 1. In this case, P_{ac} flows into the DC-link capacitor. However, this ripple frequency is relatively

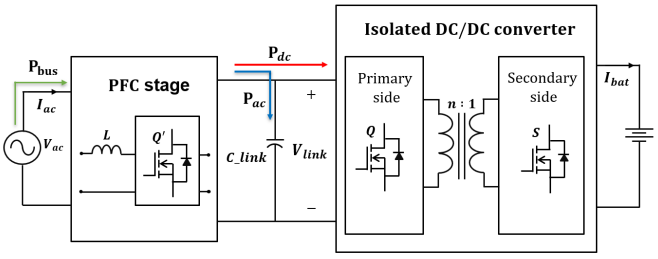


Fig. 1: Two stage onboard charger diagram.

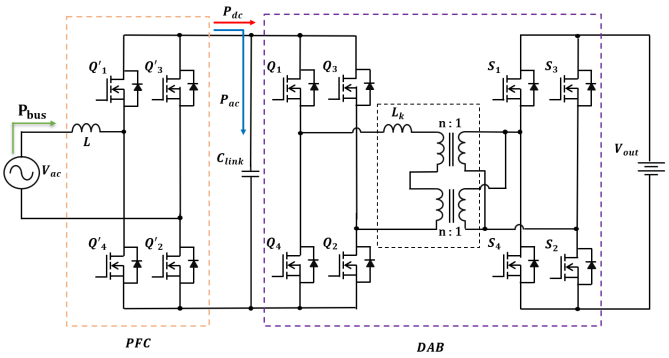


Fig. 2: General circuit diagram of the two stages on-board charger.

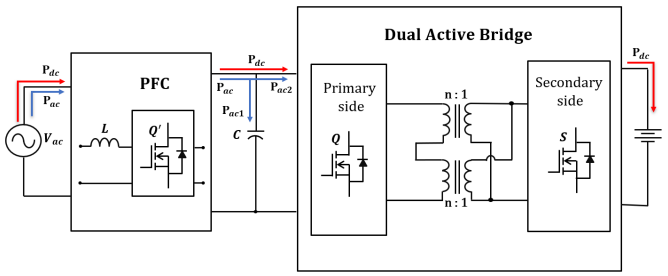


Fig. 3: Novel power flow

low (100 Hz), the DC capacitor should be large enough to reduce the DC-bus fluctuation. The power density is then reduced.

The novel power flow is shown in Fig. 3, in which the second stage (DAB converter) can be able to process the power at 100 Hz ripple from input port and make a flat DC current at the output side. This solution is advantageous because the DC-link capacitor can be reduced significantly. The power density and cost are then decreased.

Because the low frequency ripple is processed at the DAB stage. Therefore, Just the DAB converter are analyzed in detail. Some following assumptions are then made as follows:

- The PFC stage must able to supply the stable power input to the DAB stage.
- The switching frequency is much higher than the double line frequency. Then, the DC-bus voltage seems to be not

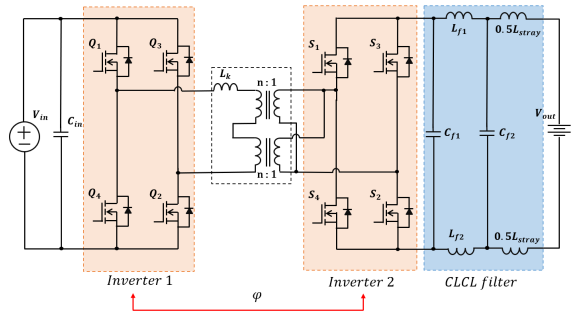


Fig. 4: Single phase Dual Active Bridge converter.

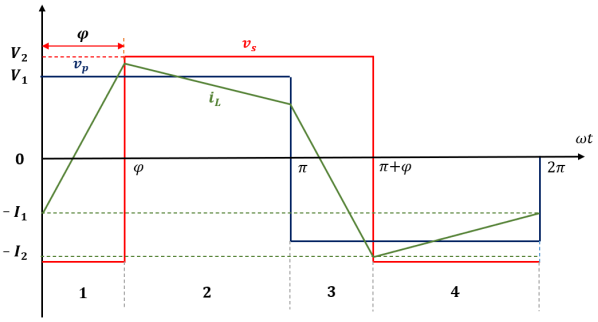


Fig. 5: Key waveforms of the DAB converter under SPS modulation.

changed in one switching cycle of the PFC converter.

B. The Dual Active Bridge Converter

Fig. 4 depicts the single-phase Dual Active Bridge converter. Two inverters are located at two side of the transformers. The MOSFETs of the primary and secondary sides are denoted as Q_x and S_x, respectively (with x = 1, 2, 3, 4). In this case, two transformers with the same turn ratio (n) are connected by the input-series and output-parallel which not only help the DAB converter can be worked effectively at high voltage gain conversion but the voltage at each transformer is also balance in nature. Moreover, the inductance is integrated to transformers as their leakage inductance. The power density is then increased. The CLCL filter, including $C_{f_1}, L_{f_1}, C_{f_2}$ and L_{f_2}, is used at the output of DAB converter. The second inductor (L_{f2}) is presented for the parasitic inductance of long capable connection in practical. The input voltage, supplied from PFC stage, is denoted as V_{in}, and the output voltage is V_{out}.

In this paper, only conventional single phase shift modulation is used to modulate to the MOSFETs of primary and secondary sides. With SPS modulation, the duty cycle of gate signal of all MOSFETs is fixed at 0.5. In each leg, the low and high side switches are modulated complementary. Two legs at the primary and secondary are shifted 180 degrees out of phase. The leg on the secondary side is shifted in phase with the corresponding leg on the primary side, denoted as φ. Some key waveforms are shown by Fig. 5 in one period ($T_s = \frac{1}{f_s} = \frac{\omega_s}{2\pi}$). The blue and red curves are depicted the gate drive signal of the MOSFETs Q_1 and S_1. Phase current (which is the current flows to the inductor) is shown by the green curve. The phase current transition are denoted as I_x (with x = 0, 1, 2, 3).

Moreover, some assumptions are made to simplified the analysis as following:

- Series resistance of the transformer winding is ignored;
- ON resistance of the MOSFETS is ignored;
- Parameters of switches are identical;
- Parameters of transformers are identical;

The output power (P_{out}) is then determined as Equation (2)

$$P_{out} = \frac{nV_{in}V_{out}\varphi}{2\pi f_s L_k}\left(1 - \frac{|\varphi|}{\pi}\right) \tag{2}$$

Where φ is the phase shift corresponding to the power transfer P_{out}

III. Modeling Analysis of the Dual Active Bridge Converter

A. Equivalent circuit of the output of DAB converter

The output power of the DAB converter is determined by Equation (2). From that, the average value of current before the capacitor C_{f_1} can be determined by Equation (3). This equation represents the equilibrium point. Because of its non-linearity, it is necessary to perturb and linearize in order to obtain the small-signal model.

$$I_{o,DAB} = \frac{nV_{in}\varphi}{2\pi f_s L_k}\left(1 - \frac{|\varphi|}{\pi}\right) \tag{3}$$

After applying the perturbation and linearizing, Equation (4) is found by the following form:

$$I_{o,DAB} + \Delta i = \frac{nV_{in}(\varphi + \Delta\varphi)}{2\pi f_s L_k}\left(1 - \frac{|\varphi + \Delta\varphi|}{\pi}\right) \tag{4}$$

The linear equation around the equilibrium point can be obtained as Equation (5)

$$\Delta i = \frac{nV_{in}}{2\pi f_s L_k}\left(1 - \frac{2\varphi}{\pi}\right)\Delta\varphi \tag{5}$$

This equation presents the variation of the DAB output current as a function of variable phase shift ($\Delta\varphi$), and it is load independent (or equivalent with a current source). Therefore, the output port of the DAB converter can be model as shown by Fig. 6

B. Modeling the CLCL output filter and current transfer function

In order to increase the filter attenuation while maintaining the current source at output characteristic compared with the traditional LC filter. The CLCL filter includes four elements as shown by Fig. 6 in which $C_{f_1}, L_f = L_{f_1} + L_{L_{f_2}}$ and C_{f_2} are the designed parameters. The final inductance (L_{stray}) represents for the parasitic inductance of long capable connection. The transfer function of the current before ($i_{o,DAB}$) and

after (i_{out}) filter need to be found to get the system transfer function.

The transfer function of the $i_{o,DAB}$ and i_{out} can be determined by dividing the filter to sub-two ports networks. Then, Chain parameter (or ABCD parameter) [10] can be used to find the whole transfer function of these sub-cascade ports. Following [10], the Chain parameters of two simple two ports networks, shown by Fig. 7(a) and (b), are determined by Equation (6) and (7), respectively.

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{7}$$

Where Z and Y are the equivalence impedance and reluctance of the corresponding branch. v_1, i_1, v_2 and i_2 are the voltage and current of the input and output port.

From these Chain parameter of two case shown in Fig. 7, the CLCL filter in Fig. 6 can be divided by 5 sub-simple networks and expresses by Equation (8).

$$\begin{bmatrix} v_1 \\ i_{o,DAB} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ C_{f_1}s & 1 \end{bmatrix} \times \begin{bmatrix} 1 & L_f s \\ 0 & 1 \end{bmatrix} \times \begin{bmatrix} 1 & 0 \\ C_{f_2}s & 1 \end{bmatrix} \times \begin{bmatrix} 1 & L_{stray}s \\ 0 & 1 \end{bmatrix} \times \begin{bmatrix} 1 & 0 \\ 1/R_o & 1 \end{bmatrix} \times \begin{bmatrix} v_2 \\ i_{out} \end{bmatrix} \tag{8}$$

From Equation (8), the transfer function of the $i_{o,DAB}$ and i_{bat} can be easily determined be Equation (9)

$$G_{i_{o,DAB},i_{bat}} = 1/\left[C_{f_1}C_{f_2}L_f L_{stray}s^4 + C_{f_1}C_{f_2}L_f R_o s^3 + L_{stray}(C_{f_1} + C_{f_2} + C_{f_1}L_f)s^2 + R_o(C_{f_1} + C_{f_2})s + 1\right] \tag{9}$$

From Equation (3) and (9), the transfer function of the battery current (after filtered) and the control variable (φ) can be expressed by Equation (10)

$$G_{i\varphi}(s) = \frac{nV_{in}}{2\pi f_s L_k}\left(1 - \frac{2\varphi}{\pi}\right) \times G_{i_{o,DAB},i_{out}} \tag{10}$$

IV. Controller Design and Implementation of Low Frequency Ripple Cancellation

Conventionality, the DAB converter is controlled by the Proportional and Integral (PI) controller to regulate the DC voltage and current with no error at steady stead. The reason

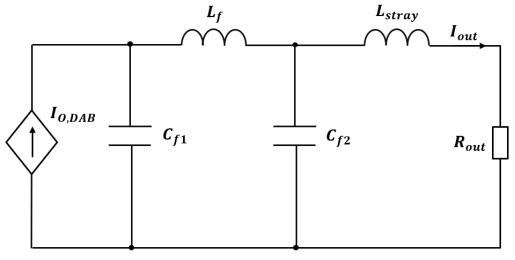
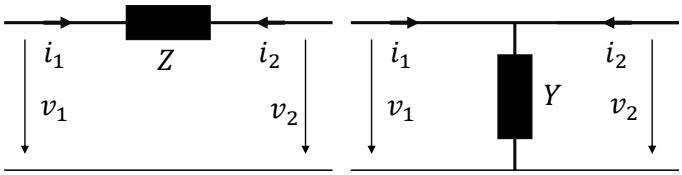


Fig. 6: Equivalent circuit of the output port of DAB converter



(a) Case 1 (b) Case 2

Fig. 7: Simple two ports networks

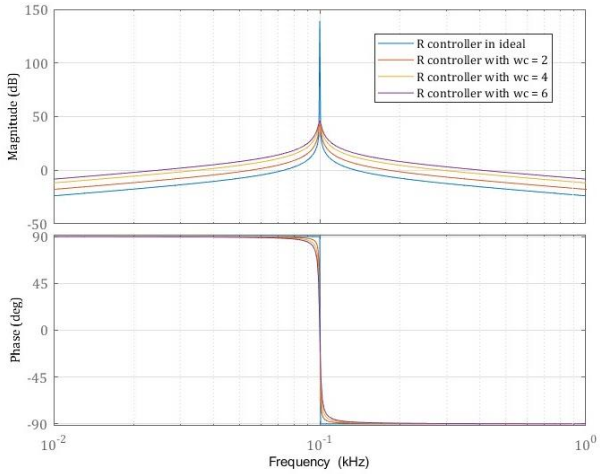


Fig. 8: Bode plot of the resonance controller

is PI controller has infinity gain at the DC (0 Hz). Therefore, in order to process the double line frequency (i.e. 100 Hz), the PI controller need to be designed at high bandwidth of current loop. It makes the gain at 100 Hz is high and the amplitude ripple of this frequency is reduced. However, the bandwidth of the current loop is limited by the low pass filter frequency and the dynamic require of the battery charging applications. For instance, the slew rate of current for battery is not exceeded 20 A/s during charging process and the shutdown slew rate must be in range if 100-200 A/s [2]. So, increasing the bandwidth to deal with the low frequency current ripple may not be a good choice.

A. R controller

As a well-known resonance (R) controller used for regulating the signal at a specific frequency. In ideally, the transfer function of R term is shown by Equation (11). This transfer function has the infinity gain at the frequency of ω_0 rad/s. Therefore, the signal having this frequency can be processed by using the R controller.

$$G_R(s) = \frac{2k_{ir}s}{s^2 + \omega_0^2} \tag{11}$$

where k_{ir} is the design parameters, and ω_0 is the resonance frequency which is double line frequency for now (100 Hz). The blue curve in Fig. 8 shows the bode plot of the ideal R controller. As mentioned above, the gain at the resonance frequency is high to eliminate the low frequency ripple. However,

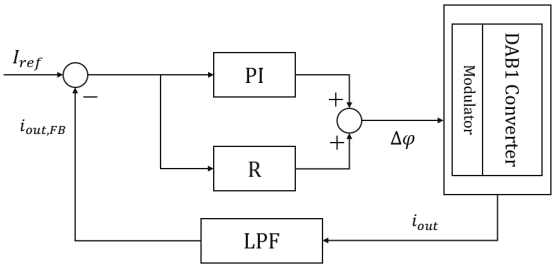


Fig. 9: Current loop controller using PI-R controller

the controller is sensitive because the gain is just high at exact resonance frequency. This means that low frequencies can still exist when there is a small error in the resonance frequency. For example, in this case, when the frequency ripple is reduced from 100 Hz to 97.5 Hz, the gain of ideal R controller is changed from 140 dB to 21.5 dB. The reduction is even more significant when increasing the mismatch between the low-frequency ripple and the resonance frequency.

To avoid this sensitivity, the modified resonance controller can be applied. Its transfer function is expressed in Equation (12). Additional parameters ω_c is used to make the R controller less sensitive than the ideal model. Three cases of the ω_c are surveyed to realize its effect to the controller. As the results show that, the peak of R controller at the resonance frequency is reduced compared with the last time, but it still remains high enough to deal with the low frequency ripple (about 50 dB). Moreover, it can be achieved relatively high gain at the frequency around resonance point. However, the ω_c should not be highly increased, because the gain is also increased. Hence, the system stability can be effected as phase margin of system is decreased.

$$G_R(s) = \frac{2k_{ir}\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{12}$$

B. Controller design with low frequency ripple cancellation

The current loop using the traditional PI controller to regulate the DC term and the modified R controller is used to process the low frequency ripple. This structure can be described by Fig. 9. Of course, the voltage loop can be still designed as a outer loop of current to operated at CV mode. However, the main concern is reducing the low frequency ripple. Hence, only the current loop parameters are designed. Then, the effective of the resonance term can be verified.

The current controller is designed for the single-phase DAB converter as shown by Fig. 4. Two transformers, integrating 30 μH leakage inductance, have the same turn ratio of 26/7. The input voltage is tested at 100 V and it is contained the 100 Hz frequency current ripple with the amplitude of 10 V. The output voltage is set at 13.6 V with the current (I_{Load} or I_{out}) is 12.5A. These parameters are summarized in Table I.

The design process can be categorized into two steps: Step 1 is designing the PI controller, and the modified R controller is added in the Step 2. As mentioned above, the load is battery with slow dynamic. The current loop is just designed at some

TABLE I: The key parameters of the DAB1 converter.

Parameters	Symbols	Value
Input voltage	V_{in}	100 VDC $\pm$ 10 Vac (at 100 Hz)
Output voltage	V_{out}	13.16 V
Output current	I_{out}	10 A
Frequency	f_s	100 kHz
Turn ratio	n	26/7
Leakage inductance	L_k	30 μH
First filter capacitor	C_{f1}	9 μH
Second filter capacitor	C_{f2}	9.4 μH
Filter inductance	L_{f1}, L_{f2}	2.5 μ H

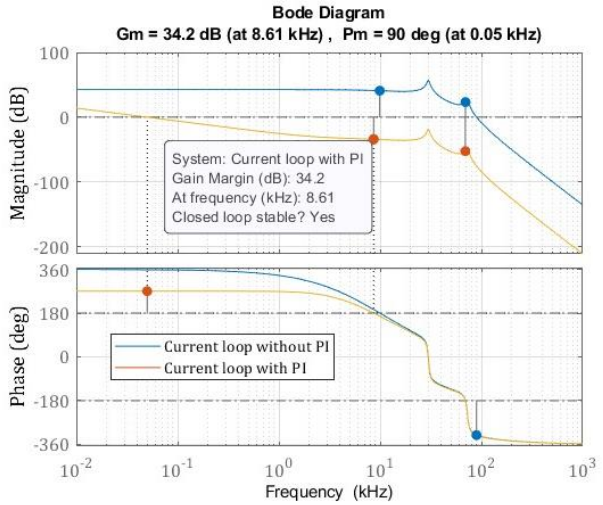


Fig. 10: Bode plot of current loop with PI controller

tens of Hz. In this case, the cut off frequency is set at 50 Hz and the phase margin is design at 90 degrees. Fig. 10 shows the results with the desired parameters as expected. The PI parameters are listed in Equation (13)

$$\begin{cases} k_p = 1.6482 \times 10^{-4} \\ k_i = 2.3402 \end{cases} \tag{13}$$

After the first step is finished, the resonance term is added in Step 2. As discuss on the Fig. 8. Although the modified resonance term can help to reduce the double line frequency ripple, it also increases the gain of system and the phase margin is then decreased. In this case, the ω_0 is kept at double line frequency (100 Hz). Let ω_c is fixed at 2 rad/s to make the controller not also be sensitive, but it also ensures high gain at the resonance frequency. Now, there is only one designed variable which is k_{ir}. Obviously, this value is used to set the desired gain at the double line frequency. For instance, k_{ir} is set to 2 to achieve about 50 dB gain at 100 Hz. The result is shown by Fig. 11.

Following [3], the bode plot may not be used when the R term is added. To ensure the system is stable when the R term is added. The Nyquist diagram of the current loop after design PIR controller is ploted and shown by Fig. 12. This graph dose not encircle the $-1 + 0j$ in the clockwise direction and there is no right half plane pole. Hence, the system must be stable.

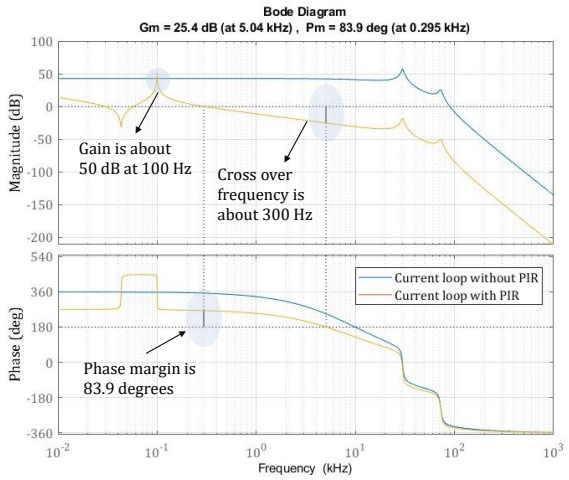


Fig. 11: Bode plot of current loop with PI-R controller

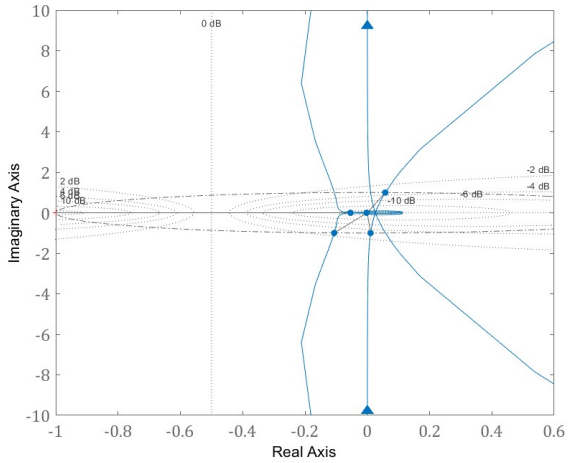


Fig. 12: Nyquist plot of the current loop with PIR controller

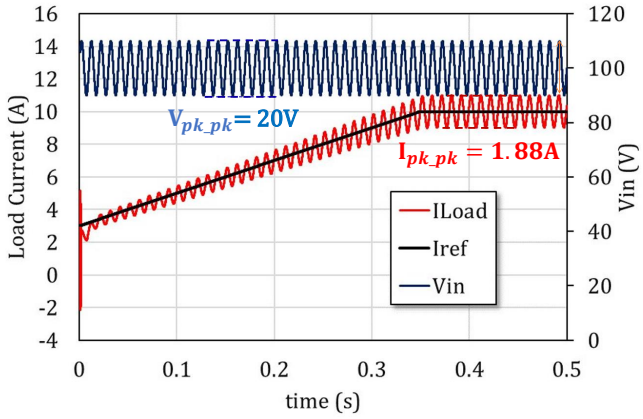


Fig. 13: Simulation result when applying only PI controller

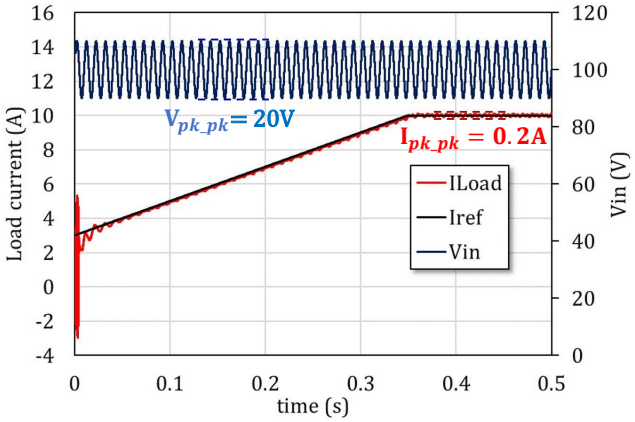


Fig. 14: Simulation result when applying PIR controller

The simulation is conducted to verified the effective of the controller. Fig. 13 describes the respond of the output current with only PI controller. The load and reference are depicted by blue and orange curve, respectively. To ensure the respond of controller can be worked in real applications, the slew rate of reference current is set to 20A/0.1s. The results show that, current is still following the reference current, but the double line frequency can be intuitively observed with the amplitude is about 1.88 A at steady state.

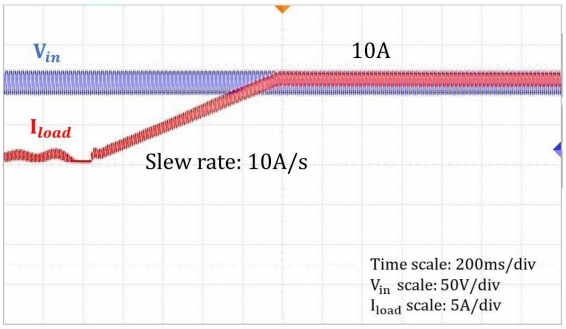
Fig. 14 shows the simulation results when the PI-R controller is applied. The color curve is the same with the previous case. As the result shows that, the current is almost flat with the ripple at 100 Hz is just about 0.2A which is more than 9 times smaller than than of the last case.

V. Experiment Results

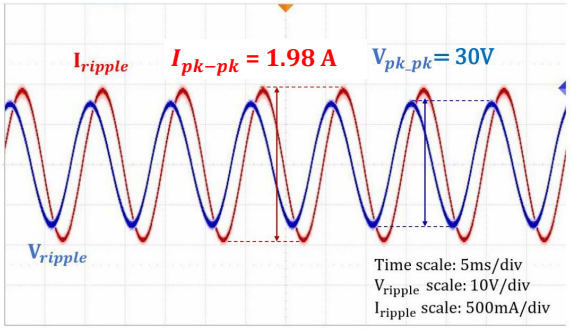
To verified the designed controller and simulations which are discussed above. The experiments are done by the hardware with the same parameters with the last simulation. Some key parameters are summarized in Table I. The input voltage is supplied by the grid simulator (Chroma 61812), which can be generate both AC and DC. The DC voltage is set at 100 V. The low frequency ripple is set to 10 Vrms at 100 Hz (twice of grid frequency). The output is connected with a battery simulator (Chroma 62000D). This load is set at the CV mode with 13.46 V. Moreover, the STM32G474RB chip from ST-MICROELECTRONIC is used to control the whole system. The parameters of PI, and R controllers are similar with the simulation. In this experiment, the current is rampped up with the slew rate of 10A/s to satisfied the IEC61851-23 standard. Then, the output current and input voltage waveforms are collected to compare the difference between before and after the designed controller is applied.

Fig. 15 shows the experiment results in case of only PI controller. The output voltage and load current is shown by red and blue curve, respectively. As result show that, the control current is exactly following 10A/s (Fig.15(a)) but the ripple is relatively high with about 1.98 A (Fig. 15(b)) as expected by simulation.

When the PIR is applied, the experiment results are collected and shown by Fig. 16. Although the input is the same with the previous case, the current is significantly smoother

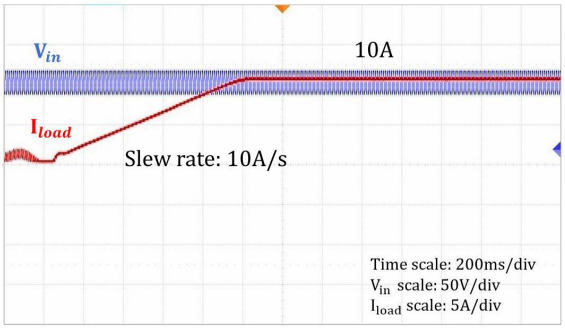


(a) The whole process

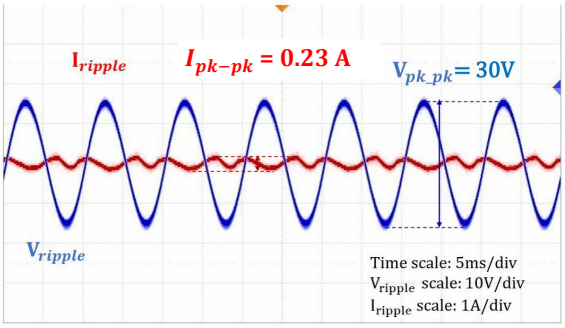


(b) Steady state with AC coupling measurement

Fig. 15: Experiment results of current with only PI controller.



(a) The whole process



(b) Steady state with AC coupling measurement

Fig. 16: Experiment results of current with PIR controller.

than before. Specifically, the double line frequency ripple is now reduced to about 0.23 A which is about nine times smaller than that of the PI case. Moreover, this results verified the simulation as shown in Fig. 13 and 14. From that, reducing the low frequency ripple by applying R term is verified.

VI. Conclusions

This paper presents the method to minimize the low frequency ripple of the output current by the software implementation. Two well-known controller, PI and R, are used. The design process are described. The results of both simulation and experiments show that, after applied the controller, the amplitude of the ripple can be reduced about 9 times compared with the before. Then, this method can be a good solution for the charging application to cancel the low frequency current ripple of the charging current.

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